

Resume of Alan J. Reiss
463 Old Connecticut Path, Wayland Mass 01778
Phone: 1-508-254-2094 FAX: 1-781-207-0393
AlanJReiss@Verizon.net

Product Specialist MSD Teradyne, Waltham Mass 1988 to 1990

Both factory and field based, responsibilities included product presentation and sales support on the L200/L300, LASAR for test and L-Series Militarized version of the Digital Test Unit. Additional activities included the creation of graphical and text presentation materials for the marketing and sales groups across all mentioned product lines, competitive analysis and presentations, Request for Proposals, descriptive product positioning summaries, specialized applications and extensive travel.. Major contributions were the creation of generalized product slide presentations and competitive presentations in which competitors were eliminated from customer consideration. Other relevant contributions were the creation of IEEE papers, nationally published article on fault dictionaries and proposal for the emulation of the MIL-STD-1553A/B bus on the L-Series timing generator. My duties also included show support and other application test solutions.

Schlumberger Corporation 1984 to 1988

Product Specialist FACTRON, Burlington Mass 1986 to 1988

The FACTRON product specialist had both pre-sales and post-sales responsibilities. Marketing slides, customer presentations, RFQ's, RFP's, show support, papers and articles and extensive travel were part of my pre-sales duties. My post-sales duties included on-site customer applications and hand-holding. The board test applications included μ P based digital PC's, asynchronous interactions, memory algorithms, time-multiplexed bi-directional bus emulations, ROM emulations, process of elimination fault diagnostics, hybrid diagnostics, mixed signal stimulus and measurement functional testing, DC analog measurements, fast-fourier transform signature analysis. FAST predictive analog in-circuit algorithms, conventional guarding for DC parametrics.

Product Manager FACTRON, Latham, NY 1984 to 1986

Introduction of series 700 into North America. Product management, positioning, pricing, GPM, sales tools, sales training, customer presentations, papers, articles, return-on-investment modeling, manufacturing scheduling.

TeleSciences Corporation 1982 to 1984

Manager of Test Engineering TeleSciences, Moorestown NJ 1982 to 1984

Justification of ATE, selection and benchmarking of ATE, setting up and managed an assembly test department. Scheduled, fixtured and completed 30 in-circuit test programs and 30 in-circuit test fixtures in 8 months. Designed and implemented a MIS for test to manufacturing feedback and quality improvement.

Chaired in design for testability review and served as liaison between design and test. Consulted on component test methodologies for linear passive analog parts. Designed Laplace Transform algorithms to test custom SIP's for lumped R,L,C values by successive frequency injection techniques. Created paper on this subject.

Functional and In-Circuit Test Engineer Consultant 1980 to 1982

Senior Test Engineer Fischer and Porter, Warminster PA

Refinement and application of authored pattern stimulus test generator on HP3060A using 9825T controller with HPL software language. Used this APG operating system to generate a number of board tests. This operating system (Static Digital Building Block Methodology) eventually became the basis for my MSEE thesis.

Test Engineer Kulicke and Soffa, Horsham PA

Developed functional test operating system using a systematic backtracing algorithm. The digital functional test (DFT) operating system was a data base driven algorithm which contained user interactive features such as topological description, auto-learn and statistical debug. The backtracing algorithm was fully documented and was used to develop tests for dozens of different PCB's.

Instructor of Computer Science 1979 to 1980

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Instructor of Computer Science Montgomery County College, Blue Bell PA
 Developed lesson plans and taught FORTRAN to 1st and 2nd year college students.

Instructor of Science 1976 to 1979

Instructor of Science Delran High School, Delran NJ
 Developed lesson plans and taught PHYSICS, CHEMISTRY and BIOLOGY to all secondary levels.

AVLSI Test Techniques Developed:

- Test Technique Note: TTN-MS-31 Teradyne Application Symposium September 1991
Digitally Synthesized Phase Modulation technique for jitter transfer testing.
- Test Technique Note: TTN-MS-XX Teradyne Application Symposium September 1992
Measuring Window Center Error Using Statistical Methods
- Integrating the LeCroy 9109 Arbitrary Waveform Generator into the A5XX. Teradyne TUG 4/93
- Test Technique Note: TTN-MS-XX Teradyne Application Symposium October 1993
Fuzzy Digital Logic Testing

Articles Published:

- High Resolution Fault Dictionary, Electronics Test Magazine, 6/90
- SuperFrame Technology, Electronics Test Magazine, 6/88
- Analog Signature Analysis - Hybrid Diagnostics EVALUATION ENGINEERING, two parts April/May 1988
- FAST-Analog Paper References, Test & Measurement World, 9/86 Article by S.Scheiber.
- High Performance Board Tester, Fault vs. Cost Economic Model. EVALUATION ENGINEERING , 8/85
- FLEXPIN and In-Circuit Tester Multiplexing Alternative ELECTRONICS magazine (Cover Story), 11/84.

Patent:

- Capturing and Evaluating High Speed Data Streams – Method for measuring random, pattern dependent and spectral jitter using a Probability Digitizing algorithm 01/08/01 01959381.3-2216-US0124086
US Patent Number 6694462 2/17/04
- Patent in process of being filed on "Relative Switching Differential Method" LTX Nov 2007

Papers Published:

- Teradyne User's Group - "GMSK Phase Detection and Modulation Techniques" - April 2000.
- Teradyne User's Group - "How to turn a uW6000 A585 into a 3GHz Spectrum Analyzer" - April 2000.
- Teradyne User's Group - "Edge Find 1999" - April 1999.
- Teradyne User's Group - "Device Firmware Management" - April 1998.
- Teradyne Applications Symposium - "Digital Statistical Sweep Parallel Jitter Technique" - January 1995.
- Teradyne Applications Symposium - "Fuzzy Digital Logic Testing" - October 1993.
- Teradyne User's Group IEEE LeCroy AWG integration to A500 Mainframe - May 1993
- Automatic Fault Injection Techniques on an In-Circuit Tester ATE Proceedings June 1989
- Behavioral Model Development using LASAR V6.4 Teradyne Users Group, 5/89 and 10/90 Paris
- Techniques in Manual and Simulation Based TPS development IEEE, ATE Boston, 6/87
- Applications in High Performance In-circuit Testing NEPCON, Boston Mass. 6/87.
- The PRIMER of Simulation and Functional Testing; an applications workshop. ATE Anaheim 1/87.
- Analog Instrumentation as integrated into functional testers. ATE Boston 6/86, IEEE Proceedings.
- Analog Functional Fault isolation without a bed of nails, a mathematical closed solution. ATE Boston 6/86, IEEE Proceedings; ATE Paris 10/86.
- An Integrated Approach to Productivity Management. ATE Boston 6/85, IEEE Proceedings.
- Surface Mounted Testing: Fixturing is not the only answer. ATE Northwest 4/85, IEEE Proceedings; ATE Boston 6/85, IEEE Proceedings.
- FAST-Analog A Re-Definition of Analog Testing. ATE Boston 6/85, IEEE Proceedings; ATE Anaheim 1/85, IEEE Proceedings.

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- A Guard Pin Contention Mathematical Model for In-Circuit Architectures. ATE Anaheim 1/85 IEEE Proceedings; ATE Northwest 4/85 IEEE Proceedings.

Sales Tools Published:

- Book: The PRIMER of High Performance In-Circuit Testing. 30,000 copies printed and distributed in USA, Europe and Japan.
- High Performance Return on Investment Spreadsheet Analysis. 10,000 copies printed and distributed USA.
- Return on Investment Slide Chart. 15,000 copies published via FACTRON USA

Industrial Education:

LTX	Fusion HFi, FX, EX Programming and Operation 2001-2005
Microsoft	Visual Basic Programming II (6/01)
Microsoft	Visual Basic Programming I (5/01)
Teradyne	Tiger Programming and Operation 8/00
Teradyne	Catalyst Programming and Operation 9/97
M5 Electronics	Synchronous Recording Channels Course (PRML) 11/95
M5 Electronics	Disk Drive Technology Course 11/95
Teradyne	A580 Programming and Operation 7/92
Teradyne	A500 High Speed Sampler Option 6/92
Teradyne	FIRMS Factory Information Management for IC Testing 2/92
Teradyne	A500 AVLSI High Speed Digital Programming 2/91
Teradyne	A500 AVLSI AC Digital Signal Processing Programming 1/91
Teradyne	A500 AVLSI DC and Basic Programming 1/91
Teradyne	Series L200/L300 In-Circuit Programming 1/89
Teradyne	Advanced LASAR Simulation 12/88
Teradyne	Introduction to LASAR Simulation 11/88
FACTRON	Series 700/730/770 In-Circuit Programming, September 1987, Latham, NY.
FACTRON	Series 700/720/750 Functional Hybrid Diagnostics, June 1987, Latham, NY.
HHB Systems	CADAT/CATS Simulation, Hardware Modeling February 1986, Mawah, NJ.
FACTRON	Series 700/720/750 Functional Combinational ATE, October 1985, Latham, NY.
FACTRON	Series 30/333 In-Circuit ATE, April 1983, Latham, NY
HP	3060A/Option 100 Functional Digital Testing ATE, March 1981, Loveland, Colo.

Total Quality Management and Improvement Training:

Teradyne	QIT Participation - Customer Service 11/92 - 5/92
Teradyne	Effective Meetings Management 11/92
Teradyne	TQM Training - QIT Participation 6/92
Teradyne	7-Steps Training and Implementation 12/91

Programming Languages:

UNIX C on PC and SUN Platforms
 Microsoft Visual Basic, Microsoft Visual Basic for Applications with extensive MS Office integration.
 RealSoftware.com RealBasic, Platforms: Unix, Linux, Windows, MacOSX

Special Skills:

Fluent Macintosh and Windows applications user including Microsoft Office extensive usage of Excel, Word, programmable data bases, VBA level MS Office programming, paint - draw - post script design software, page layout software, PC networking and connectivity, consumer routers, firewalls. Excellent typist, writing, verbal communication and teaching skills. Have given papers, workshops, seminars and formal classes worldwide.

Pubic Service

Current Member of the Board of Selectmen of Wayland, Massachusetts

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Personal Data:

Married 24 years, two children, age 54, non-smoker